IN THE SPECIFICATION:

Please amend the specification as follows:

[0030] Figure 2 is a block diagram of the receiver ~~263~~ 261 with programmable delay units (delay lines) 200 205 and a ~~serial communication port (~~configuration word interface 230~~)~~. In Figure 2, each receiver channel (220-222) includes two programmable delay units DLn1 (200, 202, 204) for input bit signal delay and DLn2 (201, 203, 205) for clock delay, and two DL registers (delay time set registers) 210 215. The DL register n1 (210, 212, 214) is for the DLn1 programmable delay unit (200, 202, 204) and the DL register n2 (211, 213, 215) is for the DLn2 programmable delay unit (201, 203, 205). The variable "n" is the channel number.

[0031] A low speed delay time configuration port 234 connected to data/clock signal line 265 is part of the configuration word interface 230. The ~~serial communication port~~ configuration word interface 230 has a shift register, a clock counter, a decoder and other control logic 232 that can implement bi-directional communications with the controller. In addition, a multiplexor 231 and phase voltage converter 233 are used in the timing adjustment. The communication instructions contain the information of chip selection, channel selection, signal or clock delay selection, delay time setting, signal-signal alignment operation, signal clock alignment operation, and so on. The ~~serial communication port~~ configuration word interface 230 is a well-known technology to those ordinarily skilled in this art field.